CLAIMS

We claim:

1. An integrated circuit comprising:

a thin film of metal oxide material; and

a hydrogen barrier layer located to inhibit the diffusion of hydrogen to said metal oxide material, said hydrogen barrier layer comprising a hydrogen barrier layer material selected from the group consisting of: strontium tantalate, bismuth tantalate, tantalum oxide, titanium oxide, zirconium oxide and aluminum oxide.

2. An integrated circuit as in claim 1 wherein said metal oxide comprises a perovskite.

3. An integrated circuit as in claim 1 wherein said metal oxide comprises a material with a dielectric constant of 20 or more.

4. An integrated circuit as in claim 1 wherein said metal oxide comprises a ferroelectric material.

5. An integrated circuit as in claim 1 wherein said metal oxide comprises a layered superlattice material.

6. An integrated circuit as in claim 5 wherein said layered superlattice material comprises one or more of the following chemical elements: strontium, calcium, barium, bismuth, lead, yttrium, scandium, lanthanum, antimony, chromium, thallium, titanium, tantalum, hafnium, tungsten, niobium, zirconium, oxygen, fluorine and chlorine.

7. An integrated circuit as in claim 6 wherein said layered superlattice material comprises a material selected from the group comprising strontium bismuth tantalate, strontium bismuth niobate and solid solutions thereof.

8. An integrated circuit as in claim 7 wherein said layered superlattice material comprises strontium, bismuth, tantalum and niobium in relative molar proportions corresponding to the stoichiometric formula $SrBi_y(Ta_{1-x}Nb_x)_2O_9$, wherein $0 \leq x \leq 1$ and $2.0 \leq y \leq 2.2$.

9. An integrated circuit as in claim 7 wherein said hydrogen barrier layer material comprises a material selected from the group consisting of strontium tantalate, bismuth tantalate, and tantalum oxide.

10. An integrated circuit as in claim 9 wherein said hydrogen barrier layer material comprises strontium tantalate.

11. An integrated circuit as in claim 1 wherein said integrated circuit comprises a capacitor having a first electrode and a second electrode, and said metal oxide material is located between said first and second electrodes.

12. An integrated circuit as in claim 11 wherein said capacitor is a ferroelectric capacitor and said metal oxide comprises a ferroelectric material.

13. An integrated circuit as in claim 12 wherein said ferroelectric material comprises a layered superlattice material.

14. An integrated circuit as in claim 1 wherein said integrated circuit comprises a field effect transistor (FET) comprising a substrate and a gate electrode, and said metal oxide material is located between said substrate and said gate electrode.

15. An integrated circuit as in claim 14 wherein said FET is a ferroelectric FET and said metal oxide material comprises a ferroelectric material.

16. An integrated circuit as in claim 15 wherein said ferroelectric material comprises a layered superlattice material.

17. An integrated circuit as in claim 1 wherein said hydrogen barrier layer is between 30 nanometers and 100 nanometers (nm) thick.

18. An integrated circuit as in claim 17 wherein said hydrogen barrier layer is between 70 nm and 90 nm thick.

19. An integrated circuit as in claim 1 wherein said hydrogen barrier layer material is amorphous.

20. An integrated circuit as in claim 1 wherein said integrated circuit includes a semiconducting substrate, and said metal oxide material is located between said hydrogen barrier layer and said substrate.

21. An integrated circuit as in claim 20 wherein said integrated circuit includes a wiring layer and a second hydrogen barrier layer located above said wiring layer.

22. An integrated circuit as in claim 1 wherein said integrated circuit further includes a substrate and a wiring layer, said metal oxide material is located between

said wiring layer and said substrate, and said hydrogen barrier layer is located above said wiring layer.

23. An integrated circuit as in claim 1 wherein said hydrogen barrier layer material comprises a primary hydrogen barrier layer material and said hydrogen barrier layer further includes a supplemental hydrogen barrier layer material different from said primary hydrogen barrier layer material.

24. An integrated circuit as in claim 23 wherein said supplemental hydrogen barrier layer material comprises silicon nitride or allumina.

25. An integrated circuit as in claim 23 wherein said supplemental hydrogen barrier layer is conducting.

26. An integrated circuit as in claim 23 wherein said supplemental hydrogen barrier layer is insulating.

27. An integrated circuit as in claim 23 wherein said supplemental hydrogen barrier layer is adjacent to and in direct contact with said primary hydrogen barrier layer.

28. An integrated circuit comprising:

a thin film of metal oxide material; and

a hydrogen barrier layer located to inhibit the diffusion of hydrogen to said metal oxide material, said hydrogen barrier layer comprising an amorphous material.

29. An integrated circuit as in claim 28 wherein said integrated circuit comprises a capacitor having a first electrode and a second electrode, and said metal oxide material is located between said first and second electrodes.

30. An integrated circuit as in claim 29 wherein said capacitor is a ferroelectric capacitor and said metal oxide comprises a ferroelectric material.

31. An integrated circuit as in claim 30 wherein said ferroelectric material comprises a layered superlattice material.

32. An integrated circuit as in claim 28 wherein said integrated circuit comprises a field effect transistor (FET) comprising a substrate and a gate electrode, and said metal oxide material is located between said substrate and said gate electrode.

33. An integrated circuit as in claim 32 wherein said FET is a ferroelectric

FET and said metal oxide material comprises a ferroelectric material.

34. An integrated circuit as in claim 33 wherein said ferroelectric material comprises a layered superlattice material.

35. An integrated circuit as in claim 28 wherein said hydrogen barrier layer is between 30 nanometers and 100 nanometers (nm) thick.

36. An integrated circuit as in claim 28 wherein said amorphous material has a crystallization temperature of greater than 650°C.

37. An integrated circuit as in claim 28 wherein said amorphous material comprises a primary hydrogen barrier layer and wherein said integrated circuit further comprises a supplemental hydrogen barrier layer that is crystalline.

38. An integrated circuit comprising:

a thin film of metal oxide material; and

a hydrogen barrier layer located to inhibit the diffusion of hydrogen to said metal oxide material, said hydrogen barrier layer comprising a primary hydrogen barrier layer material and a supplemental hydrogen barrier layer material, said primary hydrogen barrier layer material being different than said supplemental hydrogen barrier layer material, and wherein said primary and supplemental materials are either both conducting or both insulating.

39. An integrated circuit as in claim 38 wherein said supplemental material is located in contact with said primary material.

40. An integrated circuit as in claim 38 wherein said primary material and said secondary material are both conducting.

41. An integrated circuit as in claim 38 wherein said primary material and said secondary material are both insulating.

42. An integrated circuit as in claim 38 wherein said primary material is more compatible with said metal oxide material and is located closer to said metal oxide material.

43. An integrated circuit as in claim 42 wherein said primary material comprises one of the chemical elements that is in said metal oxide material.

44. An integrated circuit as in claim 43 wherein said metal oxide material is a layered superlattice material.

45. An integrated circuit as in claim 44 wherein said primary material comprises material selected from the group consisting of: strontium tantalate, bismuth tantalate, tantalum oxide, titanium oxide, zirconium oxide and aluminum oxide.

46. An integrated circuit as in claim 38 wherein said supplemental material comprises a material selected from the group consisting of silicon nitride and allumina.

47. A method of making an integrated circuit comprising:

providing a substrate;

depositing a metal oxide thin film on said substrate;

forming a hydrogen barrier layer over said metal oxide thin film, said hydrogen barrier layer comprising a material selected from the group consisting of: strontium tantalate, bismuth tantalate, tantalum oxide, titanium oxide, zirconium oxide and aluminum oxide; and

performing an integrated circuit fabrication process utilizing or producing hydrogen;

wherein said step of forming includes locating said hydrogen barrier layer in a location where it inhibits diffusion of said hydrogen into said metal oxide thin film.

48. A method as in claim 47 wherein said step of forming a hydrogen barrier layer comprises metalorganic chemical vapor deposition (MOCVD) of a liquid precursor.

49. A method as in claim 48 wherein said MOCVD is conducted at a temperature of between 300°C and 650°C.

50. A method as in claim 49 wherein said temperature is between 400°C and 500°C.

51. A method as in claim 49 wherein said temperature is 450°C or less.

52. A method as in claim 48 wherein said MOCVD is conducted at a pressure of from 1 mbar to 10 mbars.

53. A method as in claim 52 wherein said pressure is 3 mbars.

54. A method as in claim 48 wherein said MOCVD includes mixing said liquid precursor with an inert carrier gas selected from the group consisting of nitrogen and argon.

55. A method as in claim 54 wherein said inert carrier gas is argon.

56. A method as in claim 54 wherein the flow of said inert carrier gas is between 100 cubic centimeters per minute and 400 cubic centimeters per minute.

57. A method as in claim 48 wherein said liquid precursor includes an organic solvent comprising at least one compound selected from the group consisting of tetrahydrofuran, methyl ethyl ketone, isopropanol, methanol, xylene, n-butyl acetate, octane, 2-methoxyethanol, toluene, diethylethane, 1,4-dioxane and hexane.

58. A method as in claim 57 wherein said organic solvent is toluene.

59. A method as in claim 58 wherein said liquid precursor comprises a double alkoxide.

60. A method as in claim 59 wherein said double alkoxide comprises a double ethoxide.

61. A method as in claim 60 wherein said ethoxide comprises strontium tantalum penta ethoxide - 2-methoxy ethoxide.

62. A method of making an integrated circuit comprising:

providing a substrate;

depositing a metal oxide thin film on said substrate;

forming a hydrogen barrier layer over said metal oxide thin film using metalorganic chemical vapor deposition (MOCVD) of a liquid precursor; and

performing an integrated circuit fabrication process utilizing or producing hydrogen;

wherein said step of forming includes locating said hydrogen barrier layer in a location where it inhibits diffusion of said hydrogen into said metal oxide thin film.

63. A method as in claim 62 wherein said MOCVD is conducted at a temperature of between 300°C and 650°C.

64. A method as in claim 63 wherein said temperature is between 400°C and 500°C.

65. A method as in claim 63 wherein said temperature is 450°C or less.

66. A method of making an integrated circuit comprising:

providing a substrate;

depositing a metal oxide thin film on said substrate;

forming a hydrogen barrier layer over said metal oxide thin film; and

performing an integrated circuit fabrication process utilizing or producing hydrogen;

wherein said step of forming is entirely performed at a temperature of 600°C or less.

67. A method as in claim 66 wherein said step of forming is entirely performed at a temperature of 450°C or less.